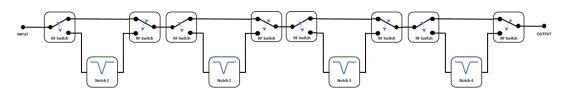


Model 5720 - Tunable Quad Notch Filter 225 - 512MHz

Block Diagram



Specifications

Frequency Range	225 to 512MHz
Notch 1 Frequency Range	225 – 299MHz
Notch 2 Frequency Range	300 - 374MHz
Notch 3 Frequency Range	375 - 449MHz
Notch 4 Frequency Range	450 – 512MHz
Notches 1, 2, 3 Rejection	15dB min at ± 2MHz
Notch 4 Rejection	13dB max at ±2MHz
Notches 1, 2, 3 Passband Insertion Loss	3.5dB max at ±24MHz*
Notch 4 Passband Insertion Loss	4dB max at ±24MHz*
Typical Notch Rejection at ±10MHz	5 - 6dB
Impedance (Input/Output)	50 Ω
VSWR	2.5:1
Temperature Range	-40°C to +85°C
RF Power Handling	+25dBm
IIP3	54dBm
DC Power	
DC Voltage	3.3 VDC ±0.3 VDC
DC Current Max	45mA
Control Interface	SPI Serial Input
Tuning Resolution	100KHz
Switching Speed, 90% RF Power (typical)	< 50µsec
Dimensions [L x W x H]	1.70 X 1.80 X 0.35 inches 43.20 X 45.20 X 8.90 mm

*Assuming other notches in bypass mode.

Note: Parameters subject to change

FEATURES

The UHF Tunable Quad Notch filter is designed with 4 independent lumped element notch filters in series.

The design topology for the filter was selected to achieve constant absolute bandwidth over the 225-512MHz frequency range.

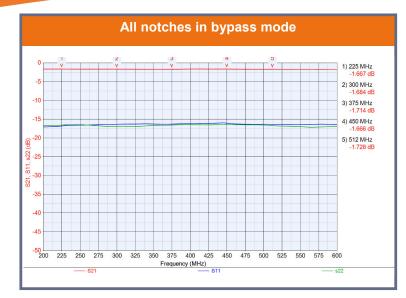
Each notch can be programmed to turn on (active mode) or off (bypass mode).

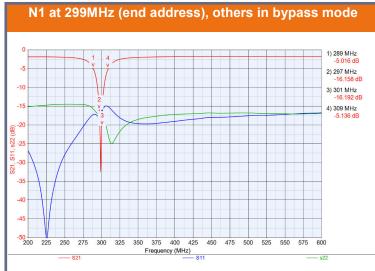
Each notch is tunable over a specific frequency range (or tuning zone). The tuning frequency step for each notch is 1MHz (tuning resolution).

The filter provides temperature control input lines to compensate the Temperature Drift of the Notch Frequency at high or low operating temperatures.



Frequency Response

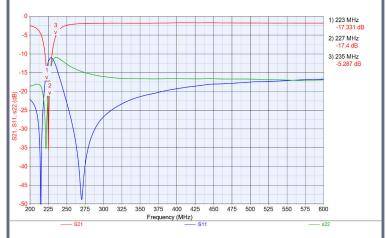




N2 at 300MHz (start address), others in bypass mode

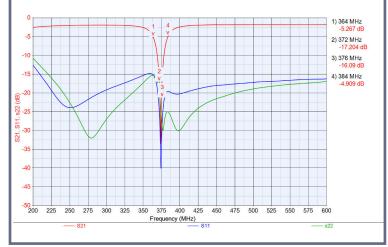


N1 at 225MHz (start address), others in bypass mode

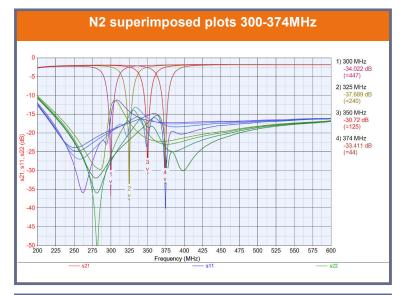


1) 225 MHz -35.694 dB (=454) 2) 249.8 MHz -25.78 dB (=214) -10 3) 275 MHz -24.269 dB (=91) 4) 299 MHz -32.506 dB (=16) S -25 s11 \$21 -35 -40 -4 -50 200 225 250 275 300 325 350 375 400 425 450 475 500 525 550 575 600 Frequency (MHz)

N2 at 374MHz (end address), others in bypass mode

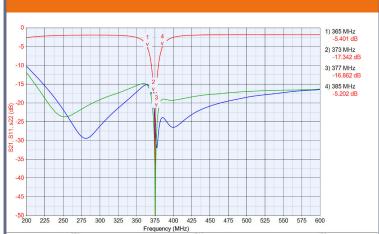


N1 superimposed plots 225-299MHz in 25MHz steps

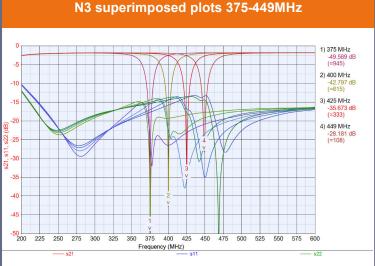


N3 at 449MHz (end address), others in bypass mode 1) 439 MHz -5.342 dB 2) 447 MHz -16.712 dB -10 3) 451 MHz -16.941 dB -15 4) 459 MHz -5.784 dB -20 8 -25 -35 -40 -4! -50 200 225 250 275 300 325 350 375 400 425 450 475 500 525 550 575 600 Frequency (MHz) - S21

N4 at 450MHz (start address), others in bypass mode 1) 440 MHz -5.225 dB -5 2) 448 MHz -16.265 dB -10 3) 452 MHz -16.182 dB -15 4) 460 MHz -4.852 dB -20 8 -25 -30 -35 -40 -45 -50 200 225 250 275 300 325 350 375 400 425 450 475 500 525 550 575 600) 375 400 Frequency (MHz) ---- \$11 - \$21 s22



N3 at 375MHz (start address), others in bypass mode



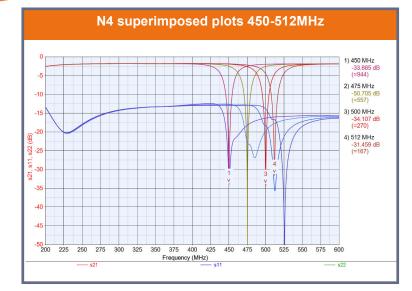
N4 at 512MHz (end address), other zones in bypass mode



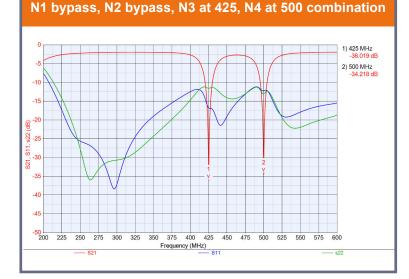
01



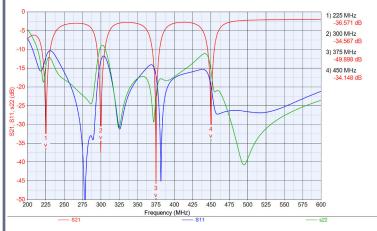
Frequency Response



N1 at 299, N2 at 374, N3 at 449, N4 at 512 combination 1) 299 MHz -33.08 dB -5 2) 374 MHz -34.16 dB -10 3) 449 MHz -28.38 dB -15 4) 512 MHz -31.779 dB -20 8 -25 S21, S11 -30 -35 -40 -45 -50 200 225 250 275 300 325 350 375 400 425 450 475 500 525 550 575 600 Frequency (MHz) 01-021



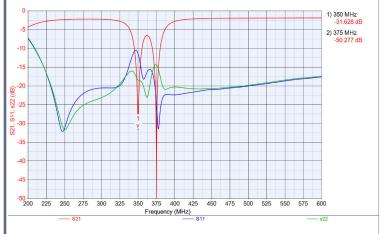
N1 at 225, N2 at 300, N3 at 375, N4 at 450 combination

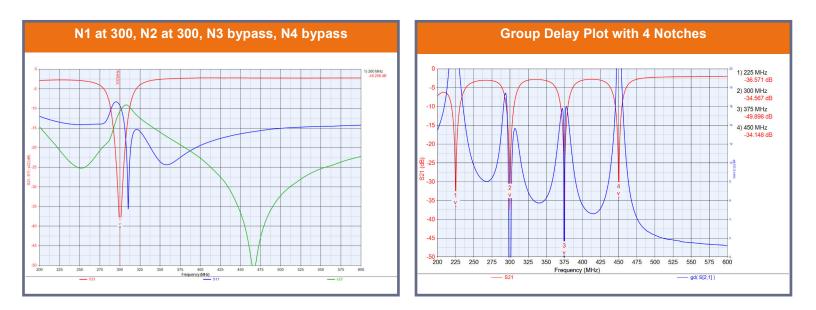


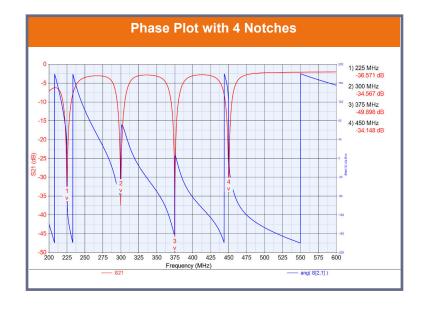




N1 bypass, N2 at 350, N3 at 375, Notch 4 bypass







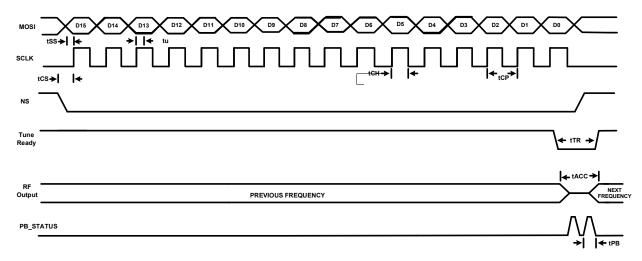
Notch(n) Serial Address Input Timing Diagram

When the SPI_NS line is shifted low, the Tune_Ready line be at a high logic state to indicate the unit is ready to accept the tune word. Tuning of the filter starts when the last data clock (16th) pulse of the address is sent to the unit while the SPI_NS (Notch Select) is low. When the filter tuning is complete the Tune_Ready line will go high to indicate the filter tuning is complete. Reset the SPI_NS line high after sending the 16th clock bit to allow the unit to reset after the filter tuning is complete.

The PB_STATUS line indicates when the filter output is disrupted by the RF Bypass switches changing state. The PB_STATUS line will go to a High logic state whenever the bypass switches change state. The PB_STATUS line will go high whenever any Notch channel is tuned to a new frequency, or a Notch channel By-pass mode is changed.

Symbol	Parameter	Min	Max	Units
tSS	Setup time MOSI Data to SPICLK	50		ns
tu	Hold Time MOSI Data From SPICLK		0	ns
tCH	Clock High Time	125		ns
tCP	Clock Period	250		ns
tCS	Chip Setup Time (CS falling edge to SPICLK start)	125		ns
tTR	Tune_Ready indicator		50	us
tACC	Access time from Last (16th) SPICLK edge to Fo		50	us
tPB	Passband Status Line Disruption at any Notch tune or Bypass Mode change instance		2.6	us

5720 ADDRESS PROTOCOL



Notch(n) Input and Output Signal Voltage Levels

Symbol	Parameter	Conditions	Min	Тур	Max	Units
FMAX	Maximum Serial Input Frequency		-		4	MHz
VIH	HIGH - level input voltage	VCC = 3.0 V to 3.6 V	1.7		VCC - 0.3	V
VIL	LOW- Level input voltage	VCC = 3.0 V to 3.6 V	-0.3		0.8	V
VOH	HIGH - level output voltage	VCC = 3.0 V to 3.6 V	2.4	3.0		V
VOL	LOW - level output voltage	VCC = 3.0 V to 3.6 V	-		0.45	V

Address Control Table

Noto	h Sele	ction						Addre	ess Sele	ection					
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB															LSB
BP*	0**	0**	Filter Tune Address***												

* 0 = Notch function Active, 1 = Notch function Bypass .** Set D14 and D13 to zero except when addressing Unit ID, Firmware Revision, or Production Date Code *** Refer to Address Table for selected notch start and end addresses.

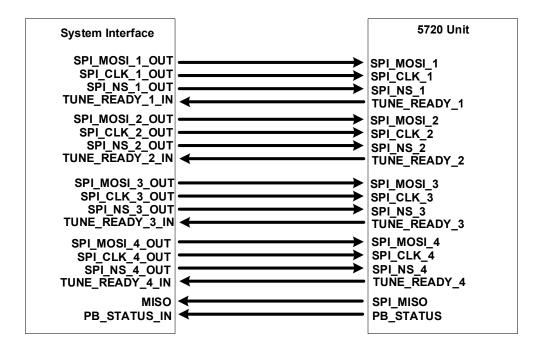
Address Table

Notch	Start Address	End Address	Frequency Range
1	2250	2999	225.0 - 299.9MHz *
2	3000	3749	300.0 - 374.9MHz *
3	3750	4499	375.0 - 449.9MHz *
4	4500	5120	450.0 - 512.0MHz *

* If address sent outside the frequency range, the filter remains in previous state

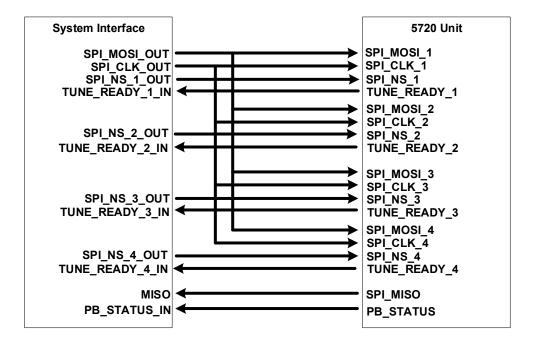
Parallel Notch Tuning Setup

- The control of the filter is through SPI interface (serial).
- The Notch Channels can be tuned simultaneously per the setup below as an example.
- Each Notch channel can be tuned to a different frequency simultaneously.



Parallel Notch Tuning Setup Common Clock and Data

- The control of the filter is through SPI interface (serial).
- The only a single Notch Channel is tuned.
- The selected Notch channel is tuned to a different frequency.



Device Commands and Addressing

The 5720 is designed to interface directly to the Serial Peripheral Interface (SPI) interface. The instructions and Addressing are listed in the table below. All instructions, addresses, and data are transferred with the MSB first and start with a High to Low transition if the SPI_NS line. Send the READ UNIT ID, READ UNIT FW CODE, and READ UNIT PRODUCTION DATE through Notch Channel 1 SPI address lines.

Instruction Name	Instruction Format	Operates On	Operation Description
Normal operation Bypass off	0000 1000 0000 0000 -		
READ UNIT ID	1011 1000 0000 0000	Unit ID Register	Read 4-digit Unit ID code (ASCII)
READ UNIT FW CODE	1101 1100 0000 0000	Unit FW Register	Read FW code 4-letter code (ASCII)
READ UNIT PRODUCTION DATE	1111 1110 0000 0000	Unit Date Register	Read 4-digit Unit Date Code (ASCII)

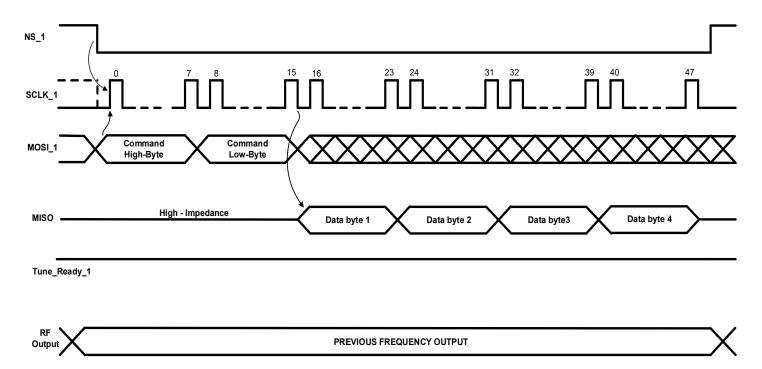
READ UNIT ID: The 5720 Quad Notch Filter will send a 4-digit ID "5720" in ASCII code when the command is sent to the unit. The unit will stay at the last Notch frequency when the command is sent.

READ UNIT FW CODE: The 5720 Quad Notch Filter will send a 4-digit Firmware ID in ASCII code when the command is sent to the unit. The unit will stay at the last Notch frequency when the command is sent.

READ UNIT PRODUCTION DATE: The 5720 Quad Notch Filter will send a 4-digit date in MMYY format in ASCII code when the command is sent to the unit. The unit will stay at the last Notch frequency when the command is sent.

Device Command Timing

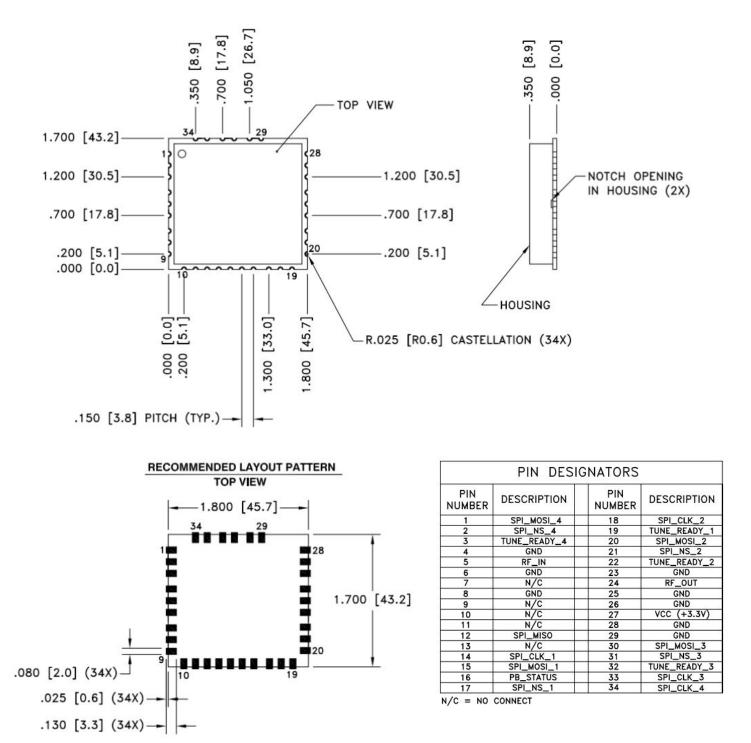
5720 READ UNIT COMMAND TIMING



The Read Unit Command Timing applies to the following commands:

- Read Unit ID
- Read Unit FW Code
- Read Unit Production Date

Mechanical



NOTES:

1. TOLERANCES ±.010 [0.25] UNLESS OTHERWISE SPECIFIED.

2. DIMENSIONS ARE INCHES [mm].

Environmental Specification Standards

Lead Plating:

• ELECTROLESS NICKEL, TYPE 1, CLASS 1, Cu/NI P7, 100 MICRO INCHES (0.0001 INCHES) MINIMUM, IMMER-SION GOLD PLATE 2 TO 6 MICRO INCHES (0.000002 TO 0.000006 INCHES) ON OUTER LAYERS.

Temperature:

- High temperature shall meet MIL-STD-810E, Method 501.3, Procedure I to 85°C storage, and procedure II to 85°C operating.
- Low temperature shall meet Method 502.3, Procedure I to -57°C storage, and Procedure II to -40°C operating.

Vibration:

• MIL-STD-810E Method 514.4 Ground Mobile Test Procedure I, Test Condition I - 3.4.7

Shock:

• MIL-STD-810E Procedure I, Method 516.4 - Functional Shock.

Reflow:

• 230°C 15 seconds [max]

Cleaning:

- Recommend cleaning solvents used which meet ODC (Ozone Depleting Chemical) requirements.
- Solvents containing methylene chloride or other epoxy solvents should be avoided since these will attack the epoxy encapsulation material of some components.
- Ultrasonic cleaning not recommended.

Moisture Sensitivity Level:

• MSL 3

REVISION CONTROL

Date (if applicable)	REV. (if applicable)	Notes / Changes
12-09-2020	-	Changed READ ID address from "1011 0100 0000 0000" to "1011 1000 0000 0000"
12-09-2020	-	Address Control Table Filter Tune Address modified from "D9-D0" to "D12-D0".
12-09-2020	-	Address Control Table BP, TC1, and TC0 moved from "D12-D10" to "D15-D13".
12-09-2020	-	Address Table addresses modified to allow 100KHz resolution.
04-19-2021	-	Changed Temperature compensation code "11" to Do Not Use
04-27-2021	-	Removed Temperature compensation chart, unit temperature correction built within unit
04-27-2021	-	Changed Address Protocol to eliminate temperature compensation bits
6-22-2021	-	Added Signal Voltage Level Table
6-22-2021	-	Removed Hop rate from Serial Address Timing Table



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