

Model 5590 - Tunable Filter 30 - 520MHz

Specifications



Frequency Range		30 to 520 MHz				
Input / Output Impedan	ce	50 Ω				
RF Power Rating						
Inband, Continuous	3		2 W			
Out-of-Band, Max			8 W			
Filter Bandwidth, 3 dB		3 %	5 %	7 %		
Insertion Loss (Typical)		5.5 dB	4.1 dB	3.3 dB		
Insertion Loss (Max)		6.8 dB	5.0 dB	4.5 dB		
Selectivity ±5%	- typical - min	13dB /10dB	9dB /7dB	6dB /5dB		
Selectivity ±10%	- typical - min	24dB /21dB	18dB /15dB	16dB /13dB		
Inband Third Order Inte	ercept Point, Min	+42 dBm				
VSWR (Max)		2:1				
Tuning Interface		100 kHz Steps				
Switching Speed, 90%	RF Power (typical)	35 µsec				
DC Inputs						
+5 Volts (±0.5 Volts	3)	300 mA				
+150 Volts (-7, +25	Volts)	5mA				
Temperature Range		-40 to +85°C				
Control Interface (User Specific Inter	face Available upon Request)	- Selectable 13 bit Parallel or Serial - TTL and CMOS Compatible				
Power Save Mode		Programmable				
RoHS Compliance		Yes				
Dimensions		2.80 x 2.00 x 0.50 inches				

FEATURES

Netcom's 5590 is a digitally tunable filter covering the frequency range of 30MHz to 520MHz.

The filter has been designed using three bands of tunable filters from Netcom's proven 5500 Series. This tri-band filter is offered in a smaller integrated SMT package to support applications where compact design, power requirements and board layout flexibility are important. It meets the vibration and shock requirements of systems used in groundmobile and airborne environments.

The following table shows the typical performance of the filter at different 3dB bandwidths. Options are available upon request for different bandwidths, insertion loss, interface step size and frequency bands.

Performance at 30MHz and 90MHz

The following plots show typical performance of a filter with a 3% bandwidth at different tuning frequencies. Across the 30 to 520MHz frequency range, insertion loss will average 5.5 dB.



Performance at 225MHz and 512MHz

The following plots show typical performance of a filter with a 3% bandwidth at different tuning frequencies. Across the 30 to 520MHz frequency range, insertion loss will average 5.5 dB.



Programming Filter Frequency Formula

5588 and 5590 tunable filter tuning control is with a 13-bit frequency word programmed into the filter. The tuning word can be entered into the filter using either serial or parallel interface.

The 13-bit frequency word is the desired filter frequency in increments of 100kHz:

FRQ WORD $_{10} = \frac{\text{Desired Frequency}}{100,000}$

The resulting frequency word ranging from 300 (30MHz) to 5200 (520MHz) is rounded to the nearest integer and converted to binary with LSB at A0 and the MSB at A12.

The table below shows an example of three programmable frequency settings for the logic levels on the address lines coming from the DIO interface. Zero in any address A0 to A12 represents a Logic 0 voltage at the DIO interface.

Frequency (MHz)	Decimal Address	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
30	300	0	0	0	0	1	0	0	1	0	1	1	0	0
200.1	2001	0	0	1	1	1	1	1	0	1	0	0	0	1
520	5200	1	0	1	0	0	0	1	0	1	0	0	0	0

PIN	REFERENCE	DESCRIPTION	MAX	PIN	REFERENCE	DESCRIPTION	MAX
1	GND		+6 VDC	15		Strobe, Falling Edge	+6 VDC
2	SCLK / A0	Serial Clock / Tune Bit A0 (LSB)	+6 VDC	16-17	GND		
3	SDI / A1	Serial Data Input / Tune Bit A1		18	Vbb	Pin Diode +150V Bias Input	+175V
4	A2			19-23	GND		
5	A3			24	RF In/Out		+33dBm
6	A4			25-33	GND		
7	A5			34-39	N/A	Factory, No connect	
8	A6			40-48	GND		
9	A7			49	RF In/Out		+33dBm
10	A8			50-52	GND		
11	A9			53	SDO	Serial Data Output	+6 VDC
12	A10	Tune Bit A2 - A12 (MSB)	+6 VDC	54	Vcc	Interface +5V Input, TTL / CMOS	+6 VDC
13	A11			55	SER/	Interface Select, 0 = Parallel	+6 VDC
14	A12			56	GND		

Note: Vbb is generated internally and has an maximum generated output of +175V

Parallel Address Input Timing Diagram

Symbol	Parameter	Min	Max	Units
tDH	Hold Time from Data to Strobe	20		ns
tSW	Strobe Dwell Time**	50		ns
tDW	Strobe Dwell Time (Strobe falling edge to next Strobe falling edge)	1000		μs
tACC	Access time from Strobe falling edge to Fo		100	μs
tSR	Setup time PAR/SER to Data	50		ns



** Filter triggers on High to Low transition of the Strobe

Serial Address Input Timing Diagram

Symbol	Parameter	Min	Max	Units
tSS	Setup time A0/Serial Data to A1/SCLK*	100		ns
tμ	Hold Time A0/Serial Data From A1/SCLK		0	ns
tCH	Clock High Time	100		ns
tCP	Clock Period	200		ns
tLH	Hold Time from A1/SCLK Serial to Strobe	100		ns
tSW	Strobe Dwell Time**	100		ns
tDW	Strobe Dwell Time (Strobe falling edge to next Strobe falling edge)	1000		μs
tACC	Access time from Strobe falling edge to Fo		100	μs
tSR	Setup time PAR/SER to A1/SCLK*	100		ns



* Data clocked in on A1/SCLK leading edge

** Filter triggers on High to Low transition of the Strobe



- 1. TOLERANCES ±0.25 UNLESS OTHERWISE SPECIFIED.
- 2. DIMENSIONS ARE mm [inches]
- Component pad plating Gold Plate over Nickel
- Units are single unit packaging.
- Suggested unit mounting to board is single unit manual soldering to board using standard settings for lead-free soldering.
- Reflow of unit is not recommended at this time.
- Product is RoHS compliant.
- Unit is considered Moisture Sensitivity Level one (MSL1) with no baking required.
- Cleaning of the unit is recommended using commercially available flux residue remover, or isopropyl alcohol based solution on bottom and sides of unit only.
- Immersion of unit not recommended.

Recommended PCB Layout

A top view of the recommended PCB layout pattern is shown below.



NOTES:

1. TOLERANCES ±0.25 UNLESS OTHERWISE SPECIFIED.

2. DIMENSIONS ARE mm [inches]

Ordering Information

Model Number	-	Bandwidth	-	Option
		3		Leave blank for selectable interface
5590		5		S: Serial Interface Only
		7		P: Parallel Interface Only



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